-1G.

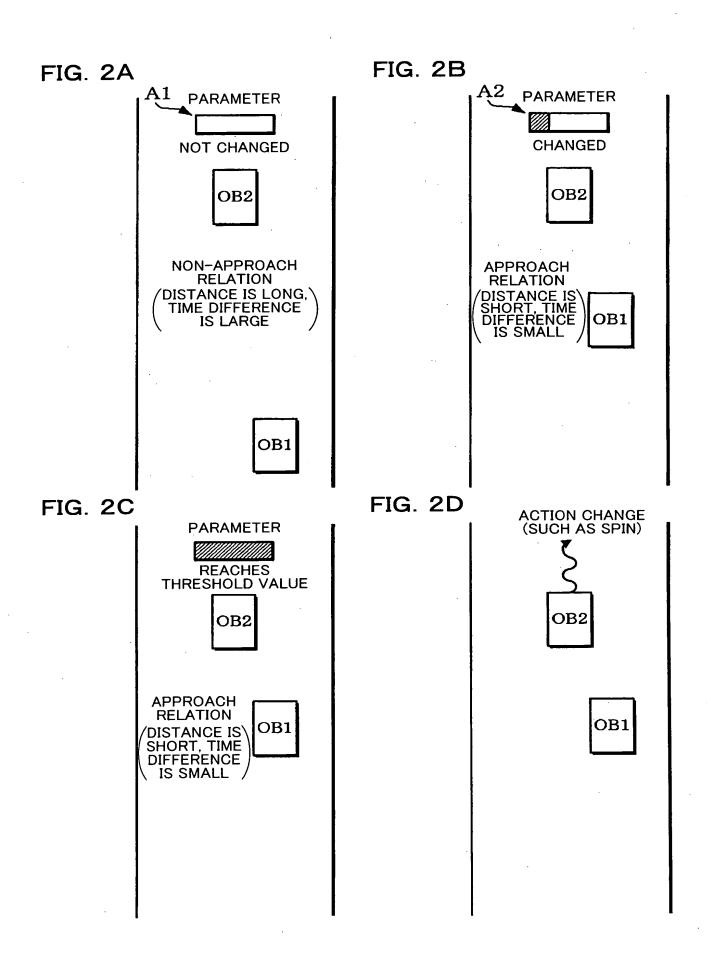


FIG. 3A

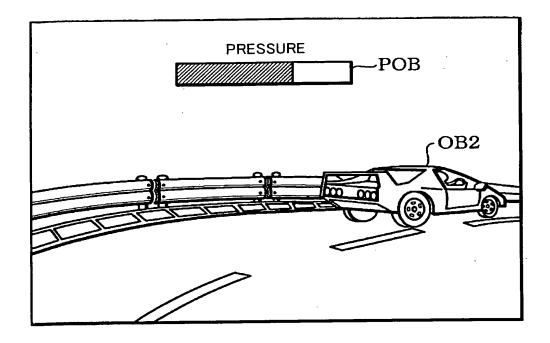


FIG. 3B

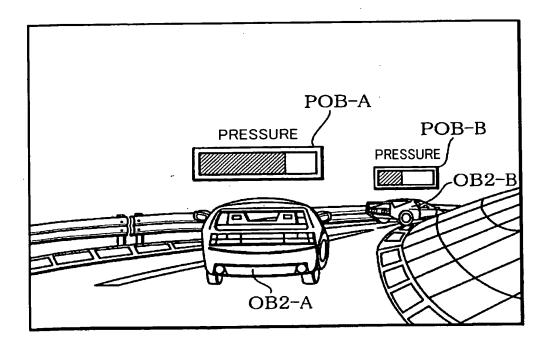
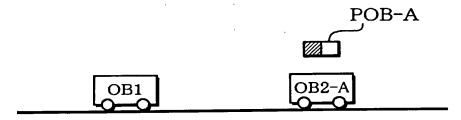
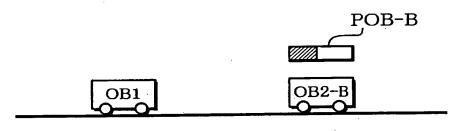


FIG. 4A



THRESHOLD VALUE: VTA
CHANGE RATE: RCA

FIG. 4B



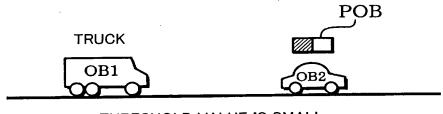
THRESHOLD VALUE: VTB CHANGE RATE: RCB

FIG. 5A



THRESHOLD VALUE IS LARGE CHANGE RATE IS LOW

FIG. 5B



THRESHOLD VALUE IS SMALL CHANGE RATE IS HIGH

PARAMETER
CHANGED

OB2

APPROACH RELATION

OB1

OB1

OB1

OB1

OB1

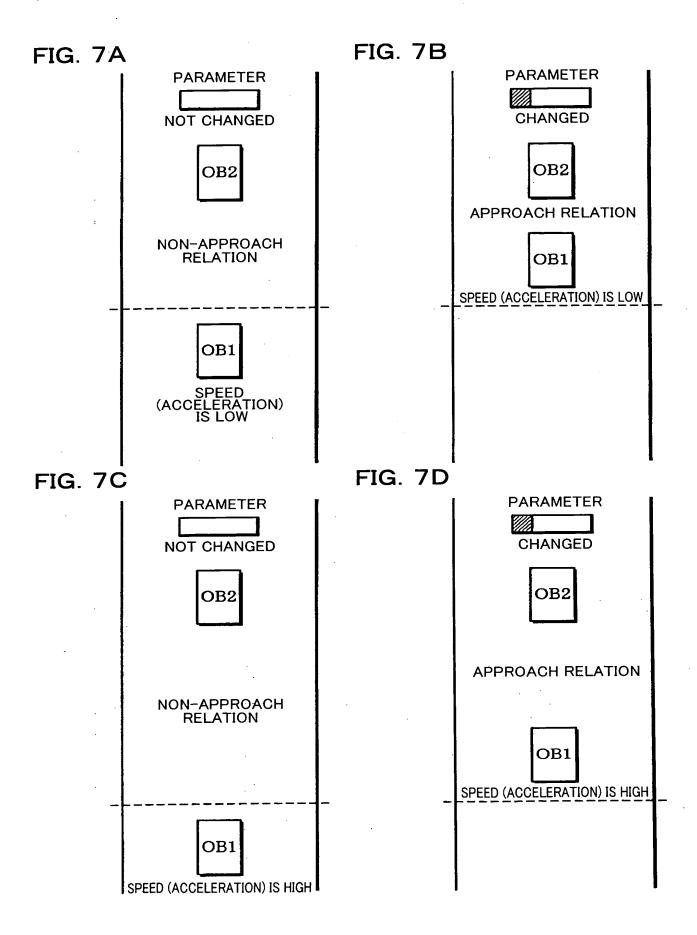


FIG. 8A

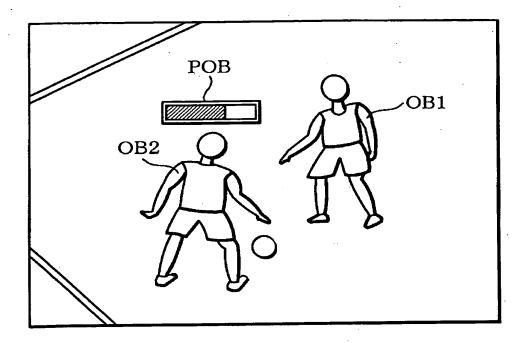


FIG. 8B

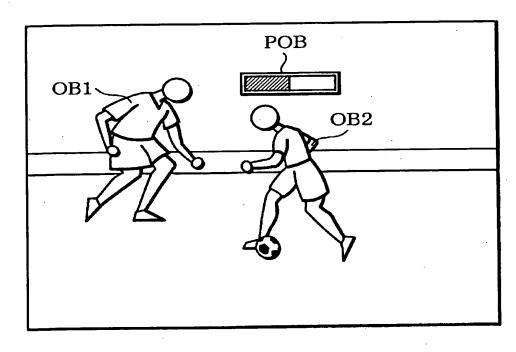
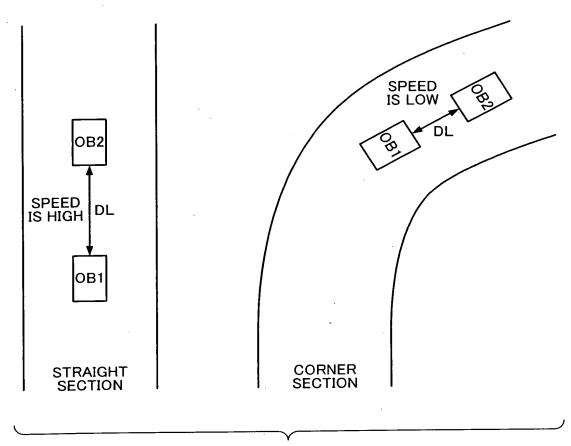


FIG. 9



CONSTANT TIME DIFFERENCE

FIG. 10A

FIG. 10B

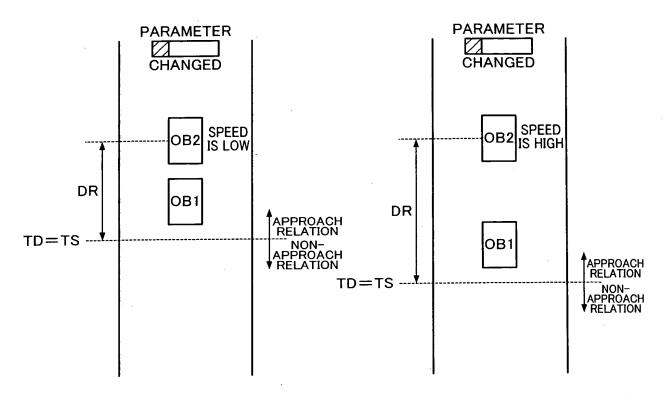


FIG. 10C

FIG. 10D

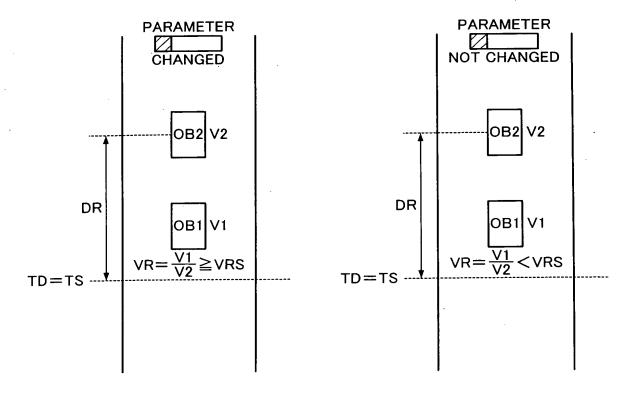


FIG. 11A

FIG. 11B

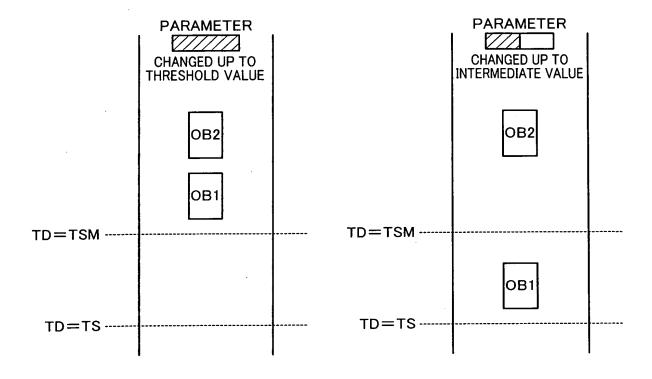
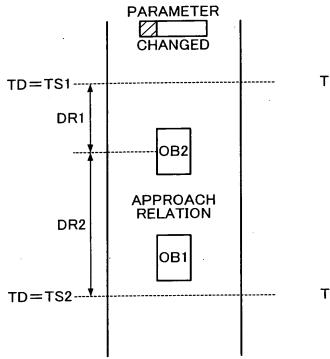


FIG. 12A

FIG. 12B



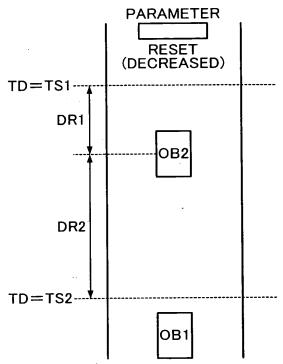


FIG. 12C

FIG. 12D

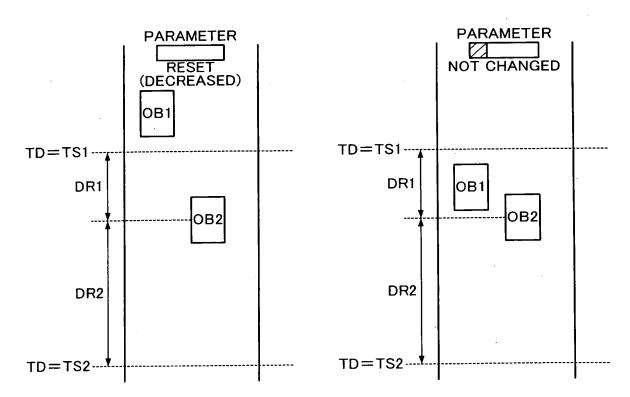


FIG. 13B FIG. 13A PASSES OB2 PASSES OB2 OB1 OB1 TRAVELING DIRECTION TRAVELING DIRECTION Z Z X FIG. 13D FIG. 13C **PARAMETER PARAMETER** CHANGE RATE IS HIGH CHANGED OB2 ОВ2 DR3 DR3 OB1 OB1

TD=TS3----\(\frac{1}{2}\)

TRAVELING DIRECTION

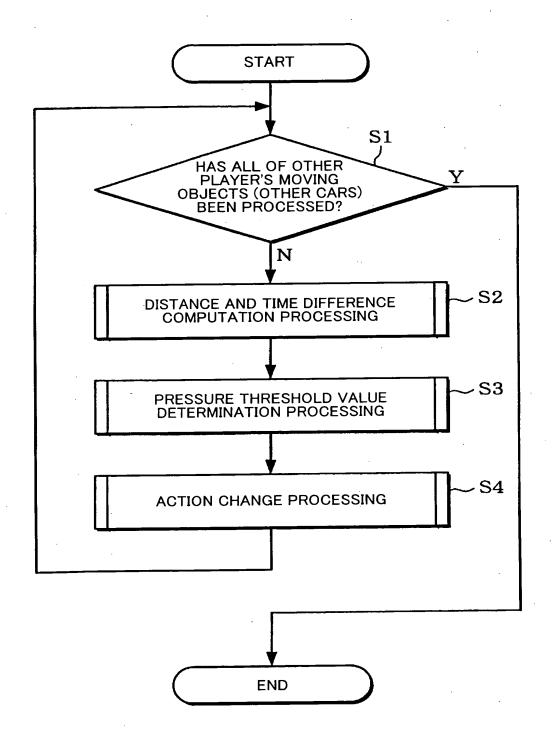
Ζ

TD=TS3----₹

TRAVELING DIRECTION

Ζ

FIG. 14



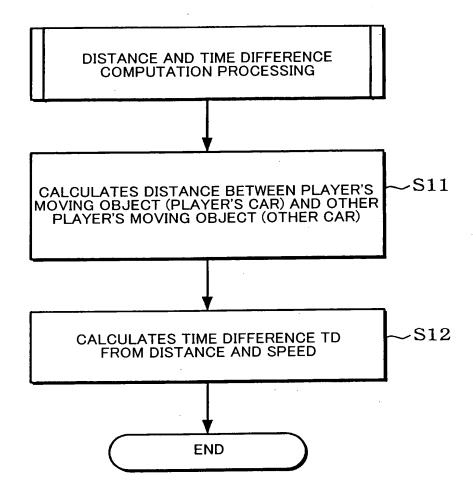


FIG. 16

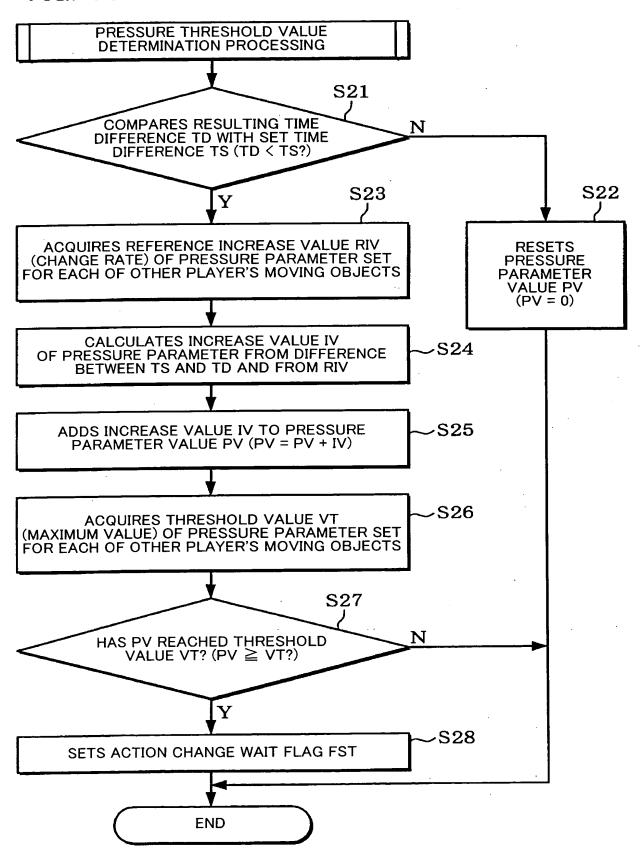
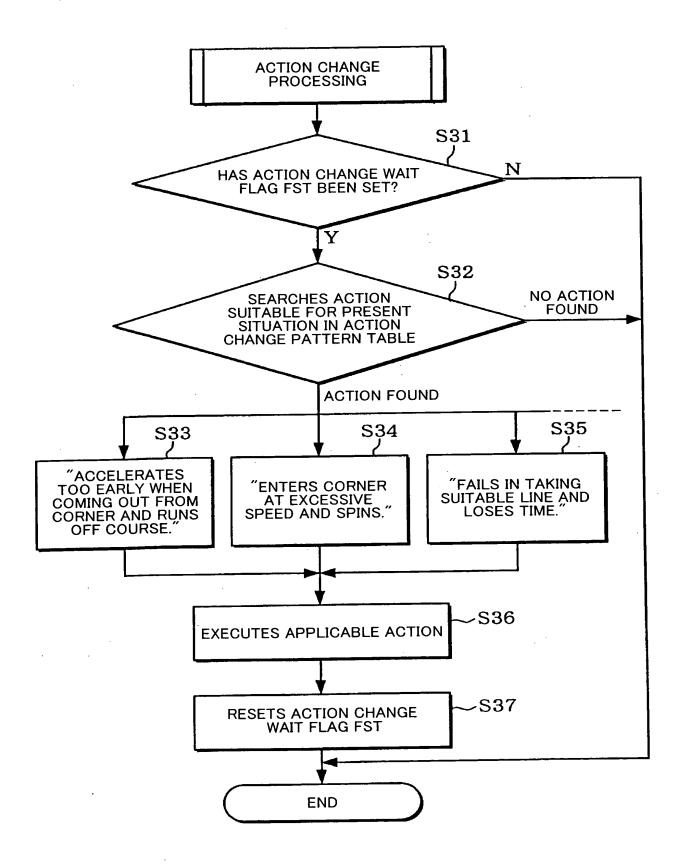


FIG. 17



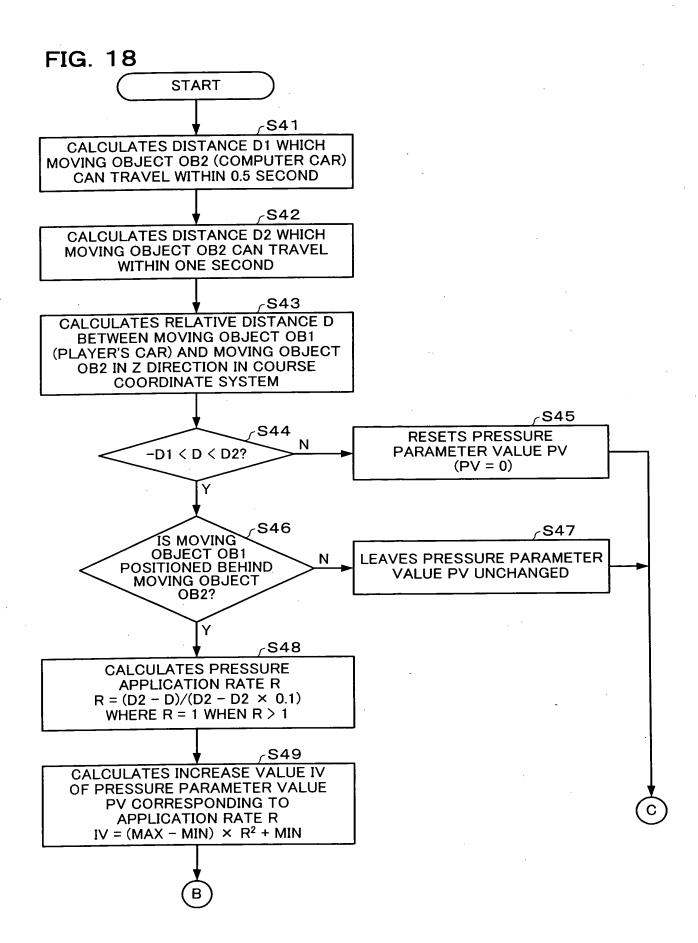


FIG. 19

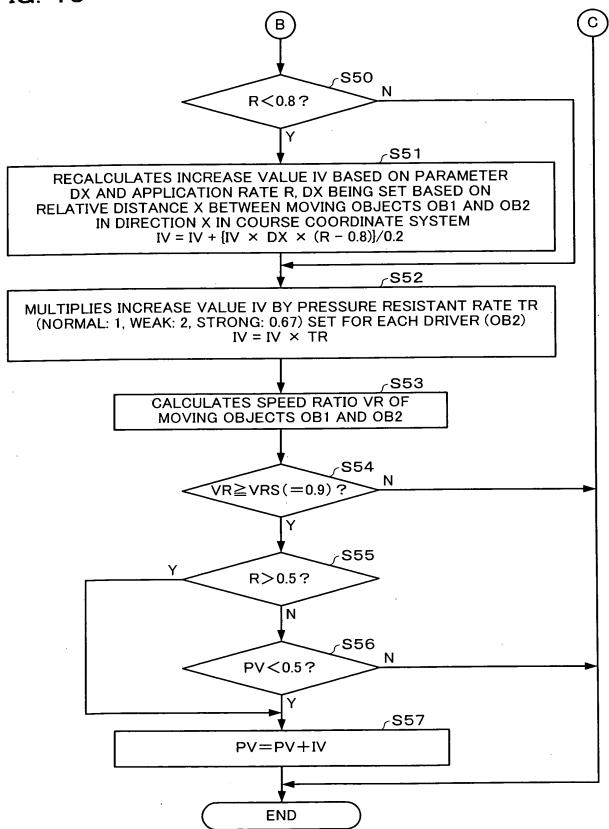


FIG. 20A

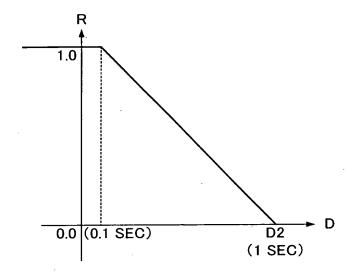


FIG. 20B

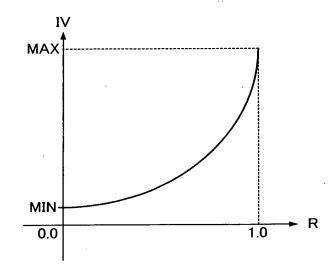
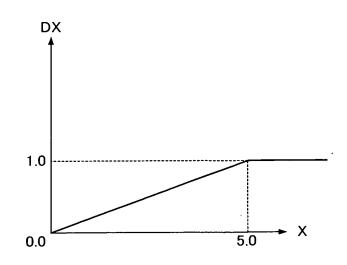


FIG. 20C



SOUND PROCESSOR CD DRIVE 970 DMA CONTROLLER TEXTURE STORAGE ,920 FRAME BUFFER VRAM 924 922 096 910 DRAWING PROCESSOR 912 DISPLAY RAM 950 DATA DECOMPRESSION PROCESSOR GEOMETRY PROCESSOR 906 902 ,904 COPROCESSOR ROM 944 MEMORY CARD 940 MAIN PROCESSOR SERIAL INTERFACE 006 GAME CONTROLLER FIG. 21 942

932

930

990

086

COMMUNICATION INTERFACE

NETWORK

CD

982

